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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/767,088

01/29/2004

Andrew T. Tomerlin

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06/08/2006

MOTOROLA, INC  
INTELLECTUAL PROPERTY SECTION  
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EXAMINER

LUU, AN T

ART UNIT

PAPER NUMBER

2816

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/767,088

Applicant(s)

TOMERLIN ET AL.

Examiner

An T. Luu

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 and 29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 and 29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some\* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                        |                                                                                         |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____                                                |

### **DETAILED ACTION**

An RCE filed on 5-11-06 has been received and entered in the case. Claims 1-21 and 29 are pending.

#### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear if the limitation “data information logic”, recited on line 3 is the same as that of line 4. The limitations “ALU” and “multiplexer”, on lines 3 and 4, have similar antecedent basis as noted above.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4, 6-10 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by the Yokota et al reference (U.S. Patent 5,712,582).

Yokota et al discloses in figure 1 an apparatus comprising a variable length delay line 100, the delay line having an input and having N delay elements (D1-m) to provide a plurality of

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N delayed outputs as shown; the variable length delay line having a number of active delay elements determined by a program command (select signal); and a configurable processing array 130 receiving the delayed outputs from the active delay elements and secondary processing data (delay data), the configurable processing array comprising an array of configurable circuit elements (G1-m) wherein the configurable processing array generating a periodic output (OUTPUT) in response to each program command as required by claim 1.

As to claim 2, figure 1 shows a control processor 160 that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements.

As to claim 4, figure 1 shows a delay locked loop 100 controlling the delay of the N delay elements.

As to claim 6, figure 1 shows the configurable processing array comprising an input (output of 400) and output (output of OR gate) that can be configured under a program control (selector control and decoder 160).

As to claim 7, figure 1 shows the configurable processing array comprising a plurality of outputs (output of G1-m) that can be configured under a program control (selector control and decoder 160).

As to claim 8, figure 1 shows the apparatus comprising a plurality of configurable processing unit (G1-m).

As to claim 9, figure 1 shows the apparatus comprising a programmable logic device 160.

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As to claim 10, the apparatus comprising a programmable MUX (i.e., decoder 160) responsive to a command (delay data) to selectively enable a selected group of delay elements while disabling remaining delay elements (i.e., which tap output is selected).

As to claims 17-21, they are rejected for reciting method/step derived from the apparatus of claims 1, 2, 3, 6, 8 and 9 which are rejected as noted above.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yokota et al reference (U. S. Patent 5,712,58) in view of the Argade reference (US Patent 6,223,255).

Yokota et al discloses all the claimed invention except for disclosing details of the control processor comprising one of: data information logic in conjunction with an arithmetic logic unit (ALU), data formatting logic in conjunction with a MUX, and a MUX in conjunction with an ALU as required by claim 3.

Argade discloses in figure 4 a control processor comprising one of data information logic 424 in conjunction with an ALU 405, data information logic in conjunction with a MUX 410 and the MUX in conjunction with the ALU as required by the claim. It would have been obvious to one skilled in the art at the time the invention was made to replace the control processor 160 of

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Yokota with the control processor taught by Argade since Argade's processor would provide n-way associative caches to be used in a conventional way for general purpose computing applications.

7. Claims 5, 11, 13-16 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Yokota et al reference (U. S. Patent 5,712,58) in view of the Lee reference (U.S. Patent 5,901,190).

Yokota et al discloses all the claimed invention except for disclosing a delay element comprising a pair of series connected inverters as required by claims 5, 25 and 28.

Lee discloses in figure 4 a delay line comprising delay elements having a pair of series connected inverters (FUD1-n) as required by the claims.

It would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Lee into that of Yokota and to realize the delay as two series connected inverters.

A skilled artisan would be motivated to employ such to provide a minimized phase difference between tapped outputs.

As to claim 11, the scope of claim is similar to the combination of claims 1, 2, 4 and 5. Therefore, it is rejected for the same reason set forth above. It is noted that element 160 in figure 1 of Yokota is seen as a control processor.

As to claim 12, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 6. Therefore, it is rejected for the same reason set forth above.

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As to claim 13, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 7. Therefore, it is rejected for the same reason set forth above.

As to claim 14, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 8. Therefore, it is rejected for the same reason set forth above.

As to claim 15, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 9. Therefore, it is rejected for the same reason set forth above.

As to claim 16, the scope of claim is similar to the combination of claims 1, 2, 4, 5 and 10. Therefore, it is rejected for the same reason set forth above.

As to claim 29, the scope of claim is similar to the combination of claims 11, 12, 13 and 14. Therefore, it is rejected for the same reasons set forth above.

### ***Response to Arguments***

8. Applicant's arguments filed 5-11-06 have been fully considered but they are not persuasive.

Regarding the rejections of claims under 35 USC 102, Applicant has argued that *"Applicant's delay line 10 does not change based on the reconfiguration. Yokota's input to delay line (120), on the other hand, does change in response to the reconfiguration because of the feedback path, as seen in FIG. 1. Applicants' input 24 to delay line 10 and data out 42 are not tied together (no feedback) and are thus structurally distinguishable from the Yokota reference."* Examiner respectfully disagrees with Applicant's argument since it is irrelevant with respect to the recitation of claim. The recitation of claim of the instant application merely calls for *"the configurable array generating a periodic output in response to each program command"*.

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Therefore, if *Applicants' input 24 to delay line 10 and data out 42 are not tied together (no feedback)* is completely irrelevant with respect to determination merit of claim.

### ***Conclusion***

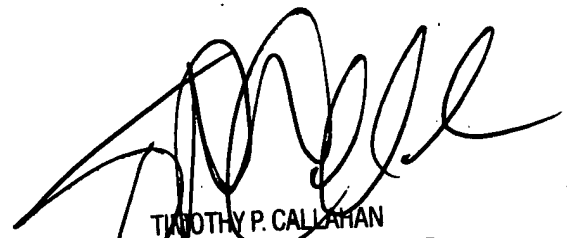
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to An T. Luu whose telephone number is 571-272-1746. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

An T. Luu  
5-18-06 *ATL*

  
TIMOTHY P. CALLAHAN  
SUPERVISORY PATENT EXAMINER  
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